ESE545: Computer Architecture
Spring 2014

Description:
This course focuses on the techniques of quantitative analysis and evaluation of modern computer systems. The emphasis is on instruction set design, pipelining, instruction-, thread-, and data-level level parallelism, and memory hierarchies. Students will undertake a design project on the dual-issue multimedia processor design related to the course contents. The project is to be done with a use of hardware description languages, such as VHDL or Verilog, as well as modern CAD systems, such as Cadence, Mentor Graphics, etc.

Course Designation: Required for CE


Instructor: Mikhail Dorojevets

Goals: To give students in-depth understanding of key architectural techniques in designing modern digital computer systems. Using that knowledge, they will be able to design and simulate complex pipelined processors using Verilog/VHDL language and modern CAD tools.

Course Learning Outcomes: Upon completion of this course, students will learn: 1) computer performance and instruction set design principles, 2) RISC architecture, 3) non-pipelined and pipelined processor design approaches, 4) software and hardware techniques of exploiting instruction- and thread-level parallelism, 5) vector and multimedia processors to exploit data-level parallelism, 6) caches, and memory hierarchy design, and 7) multiple-issue pipelined processor design and verification using VHDL/Verilog languages and modern CAD tools.

Class/laboratory Schedule: 2 lecture hours per week.

Program Outcomes and Assessment % contribution*

✓ ability to apply knowledge of math, engineering, and science 25
✓ ability to design system, component or process to meet needs 40
✓ ability to identify, formulate, and solve engineering problems 25
✓ ability to communicate effectively 10